

Features

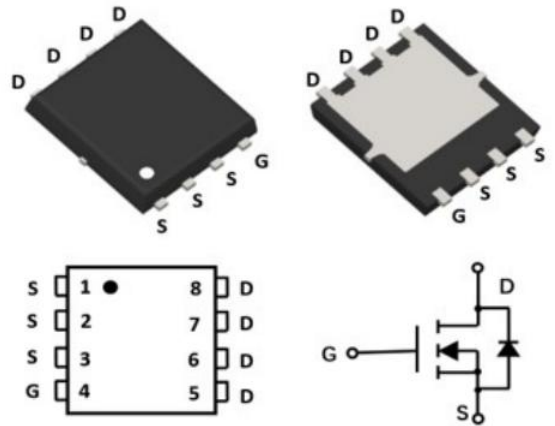
- Uses RKW advanced SGT technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- Qualified according to JEDEC criteria

Product Summary

V_{DS}	100V
$R_{DS(on),max}$	7.9m Ω
I_D	75A

Applications

- Synchronous Rectification for AC/DC Quick Charger
- Battery management System
- UPS (Uninterruptible Power Supplies)



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
HXMS100N79LNA	S100N79LNA	PDFN5X6	---	---	---	---

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	100	V
Continuous drain current $T_C = 25^\circ\text{C}$ (Silicon limit) $T_C = 25^\circ\text{C}$ (Package limit) $T_C = 100^\circ\text{C}$ (Silicon limit)	I_D	85 75 45	A
Pulsed drain current ($T_C = 25^\circ\text{C}$, t_p limited by T_{jmax})	$I_{D \text{ pulse}}$	240	A
Avalanche energy, single pulse ($I_D = 23\text{A}$, $R_g = 25\Omega$) ^[1]	E_{AS}	130	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation ($T_C = 25^\circ\text{C}$)	P_{tot}	69	W
Operating junction and storage temperature	T_j, T_{stg}	-55...+150	$^\circ\text{C}$
Soldering temperature, wave soldering only allowed at leads (1.6mm from case for 10s)	T_{sold}	260	$^\circ\text{C}$

※. Notes:

1.EAS is tested at starting $T_j = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $I_{AS} = 23\text{A}$, $V_{GS} = 10\text{V}$.

2.Repetitive rating, pulse width limited by junction temperature $T_J(\text{MAX}) = 150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J = 25^\circ\text{C}$.



Gate resistance	R_G	0	1.0	5	Ω	$V_{GS}=0V, V_{DS}=0V,$ $f=1MHz$	
Parameter					Symbol	Max	Unit
Thermal resistance, junction – case.					R_{thJC}	1.82	$^{\circ}C/W$
Thermal resistance, junction – ambient(min. footprint)					R_{thJA}	50	

Electrical Characteristic (at $T_j = 25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV _{DSS}	100	-	-	V	V _{GS} =0V, I _D =250μA
		100	-	-	V	V _{GS} =0V, I _D =1mA
Gate threshold voltage	V _{GS(th)}	1.5	2.0	2.5	V	V _{DS} =V _{GS} , I _D =250μA
Zero gate voltage drain current	I _{DSS}	- -	- -	1 100	μA	V _{DS} =100V, V _{GS} =0V T _j =25°C T _j =125°C
Gate-source leakage current	I _{GSS}	0	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
Drain-source on-state resistance	R _{DS(on)}	-	6.5	7.9	mΩ	V _{GS} =10V, I _D =30A
		-	8.6	10.5		V _{GS} =4.5V, I _D =30A
Transconductance	g _{fs}	-	93.6	187.2	S	V _{DS} =5V, I _D =30A

Dynamic Characteristic

Input Capacitance	C_{iss}	1450	2200	3300	pF	$V_{GS}=0V, V_{DS}=50V, f=1MHz$
Output Capacitance	C_{oss}	220	330	495		
Reverse Transfer Capacitance	C_{rss}	6	12	24		
Gate Total Charge	Q_G	27	41.0	61.5	nC	$V_{GS}=10V, V_{DS}=50V, I_D=30A$
Gate-Source charge	Q_{gs}	7	10.3	15.45		
Gate-Drain charge	Q_{gd}	4	7.5	15		
Turn-on delay time	$t_{d(on)}$	6	11.0	22	ns	$V_{GS}=10V, V_{DD}=50V, R_{G_ext}=2.7\Omega$
Rise time	t_r	24	36.0	54		
Turn-off delay time	$t_{d(off)}$	22	33.0	49.5		
Fall time	t_f	7	10.3	15.45		
Gate resistance	R_G	0	1.0	5	Ω	$V_{GS}=0V, V_{DS}=0V, f=1MHz$



Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.85	1.4	V	$V_{GS}=0V, I_{SD}=30A$
Body Diode Reverse Recovery Time	t_{rr}	24	47.8	95.5	ns	$I_F=30A, dI/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	36	71.0	142.0	nC	



Typical Performance Characteristics

Fig 1: Output Characteristics

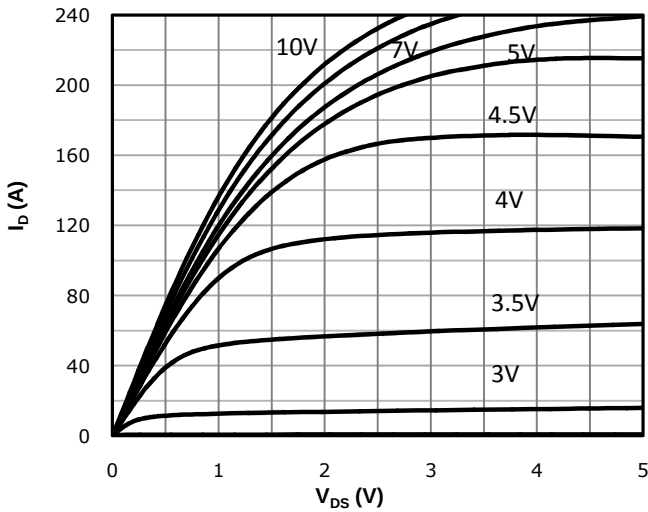


Fig 2: Transfer Characteristics

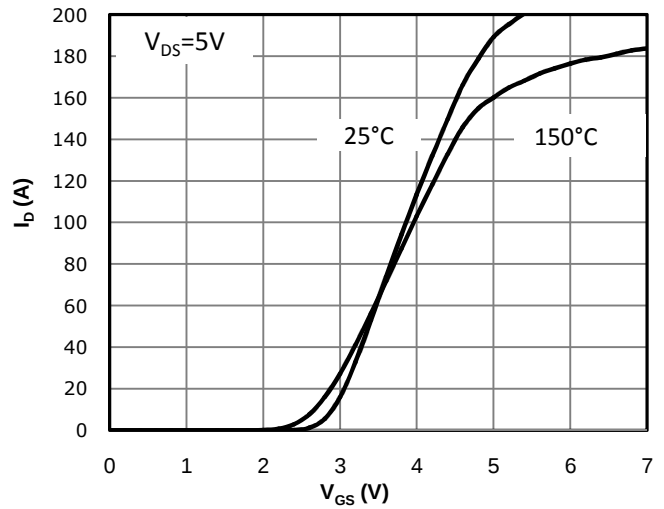


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

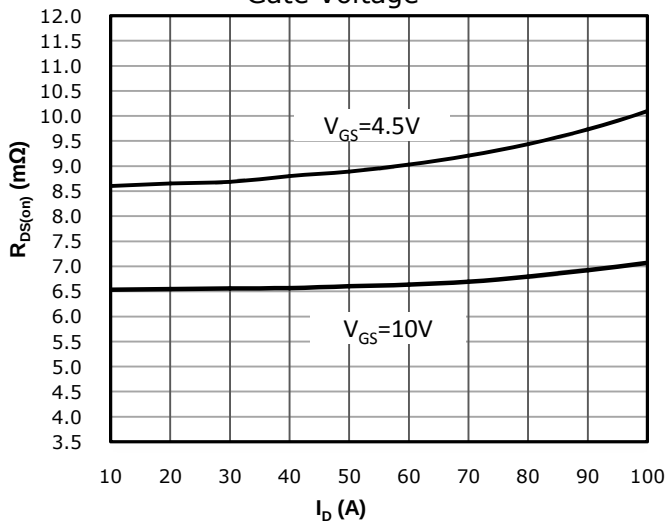


Fig 4: $R_{DS(on)}$ vs Gate Voltage

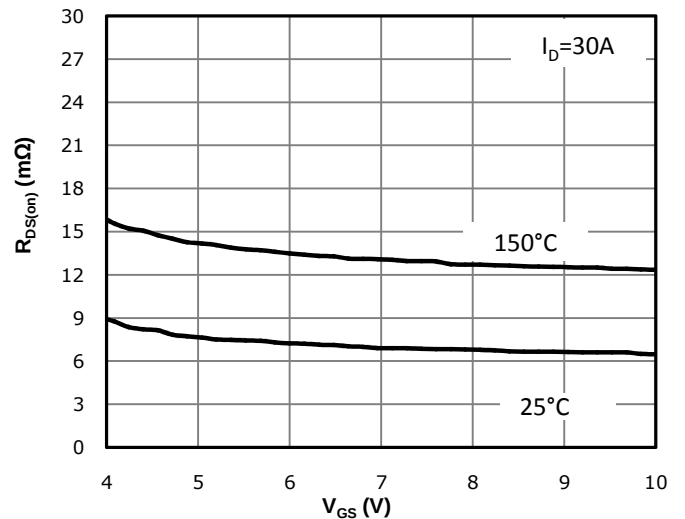


Fig 5: $R_{DS(on)}$ vs. Temperature

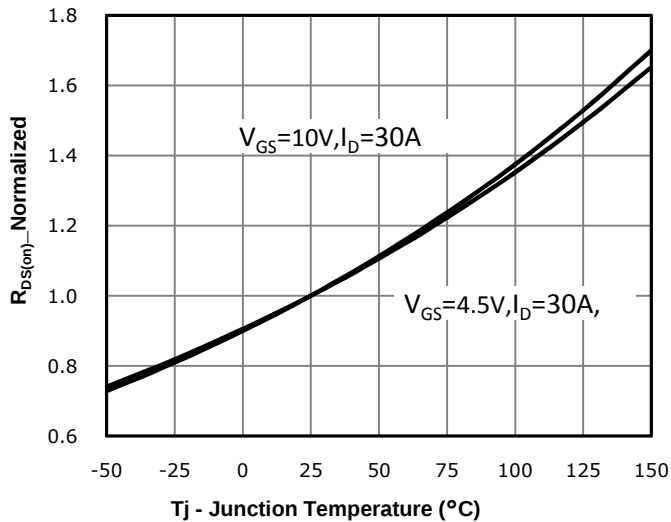


Fig 6: $V_{GS(th)}$ vs. Temperature

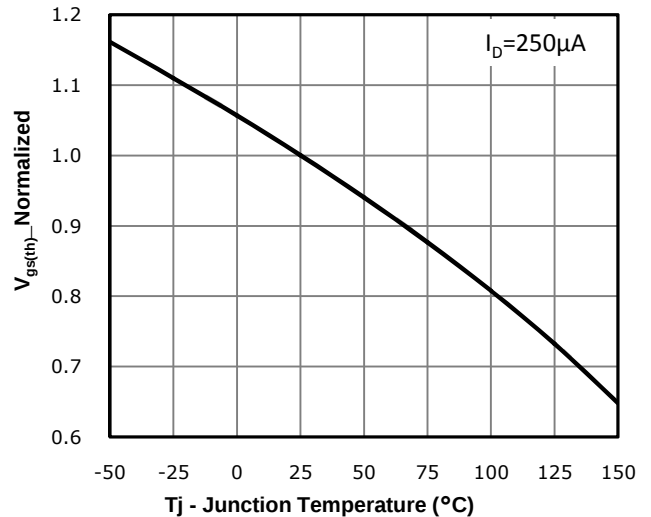


Fig 7: BVdss vs. Temperature

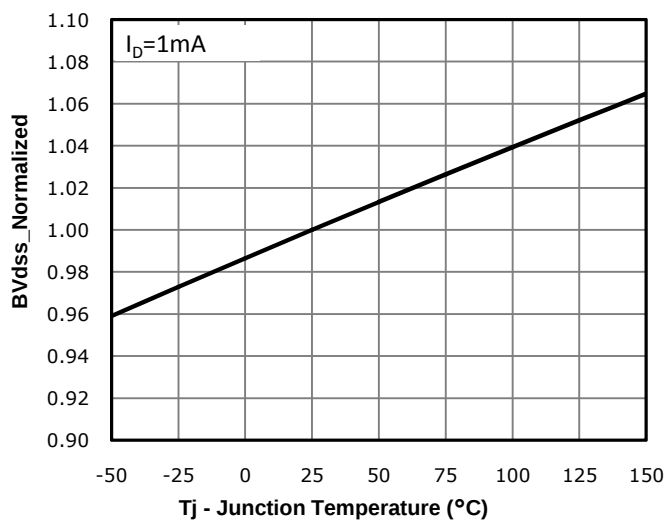


Fig 8: Capacitance Characteristics

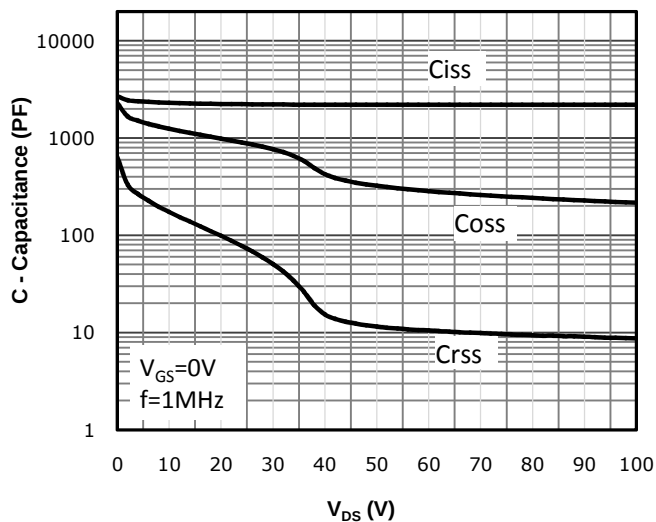


Fig 9: Gate Charge Characteristics

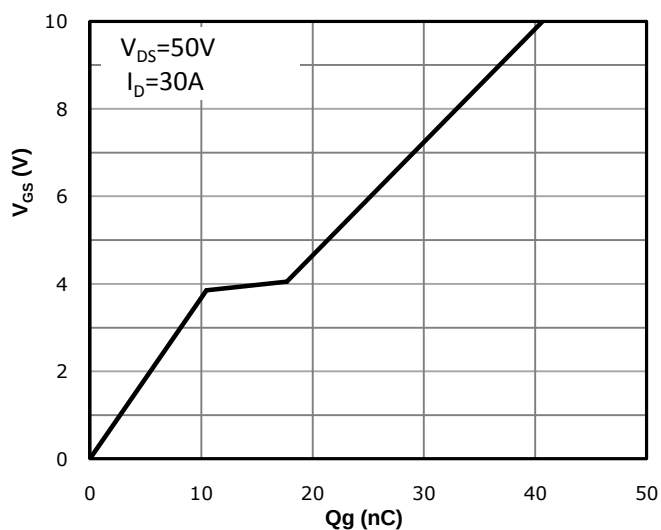


Fig 10: Body-diode Forward Characteristics

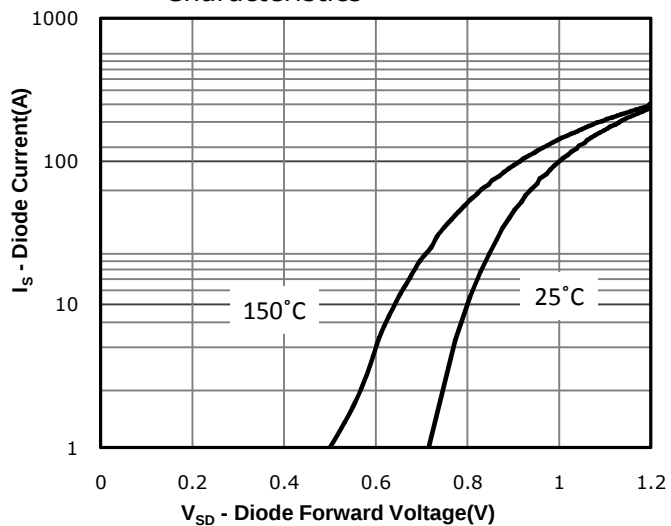


Fig 11: Power Dissipation

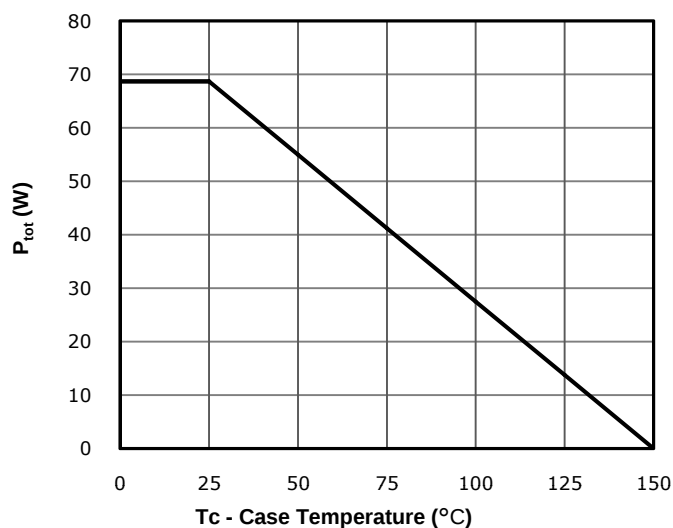


Fig 12: Drain Current Derating

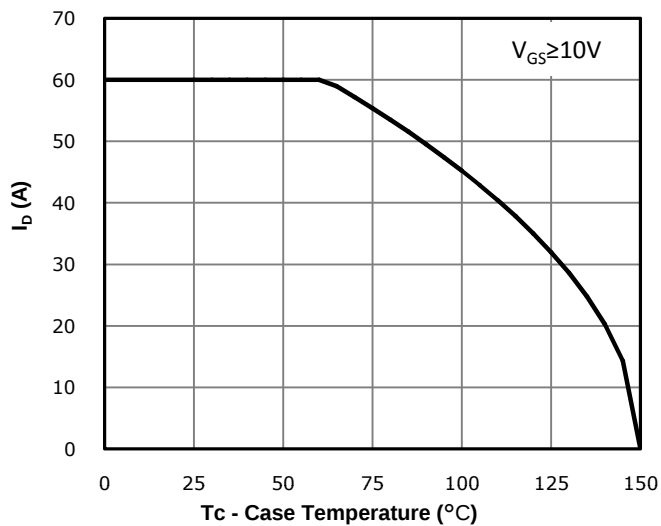


Fig 13: Safe Operating Area

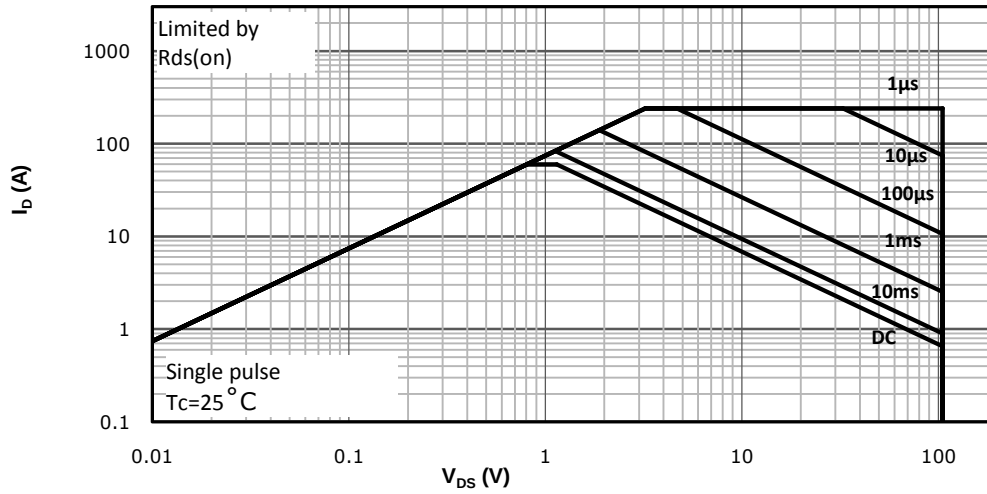
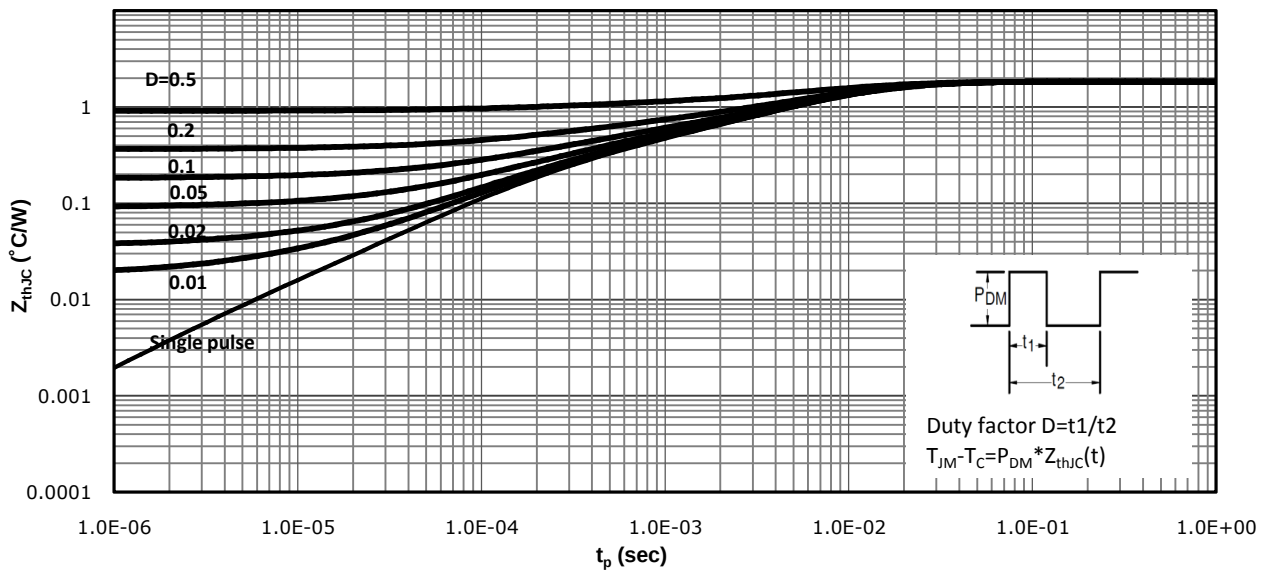
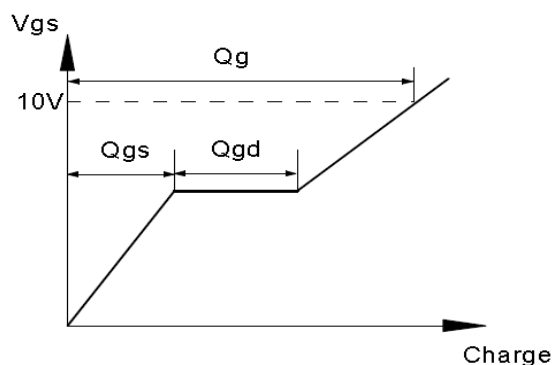
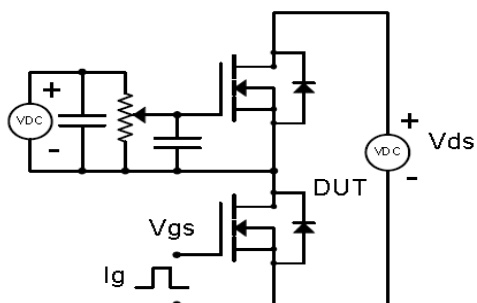


Fig 14: Max. Transient Thermal Impedance

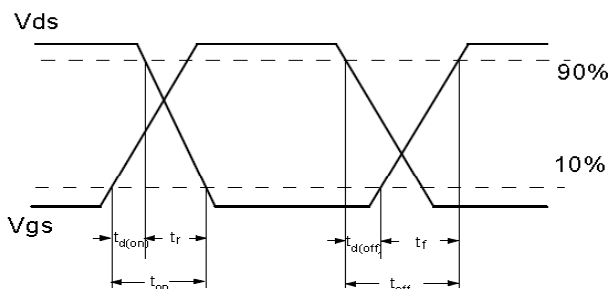
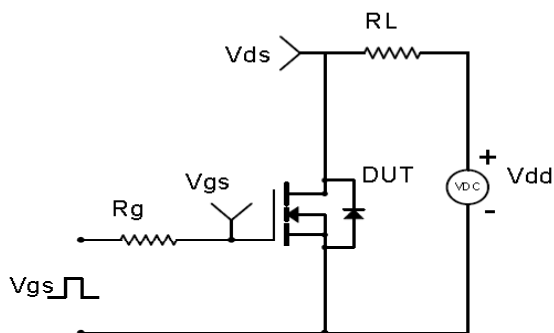


Test Circuit & Waveform

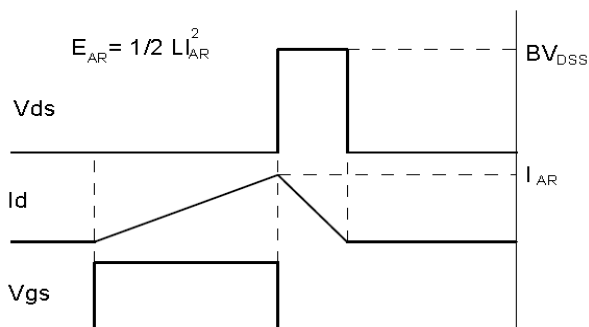
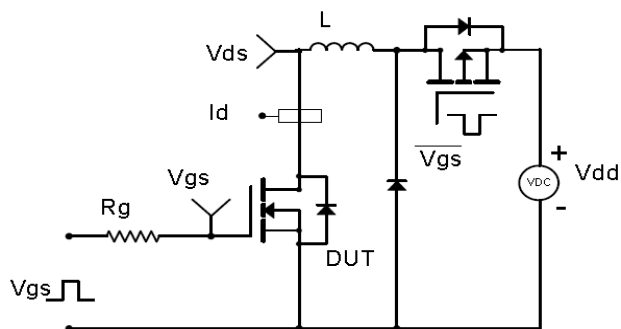
Gate Charge Test Circuit & Waveform



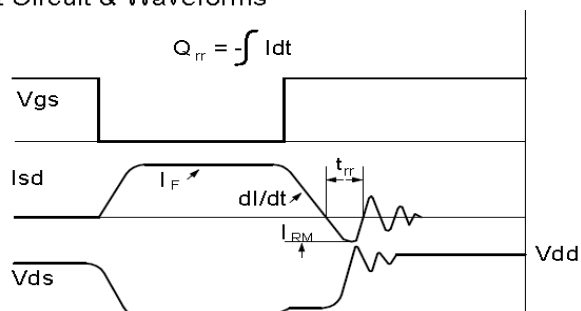
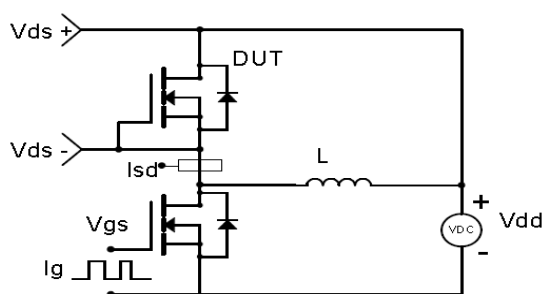
Resistive Switching Test Circuit & Waveforms



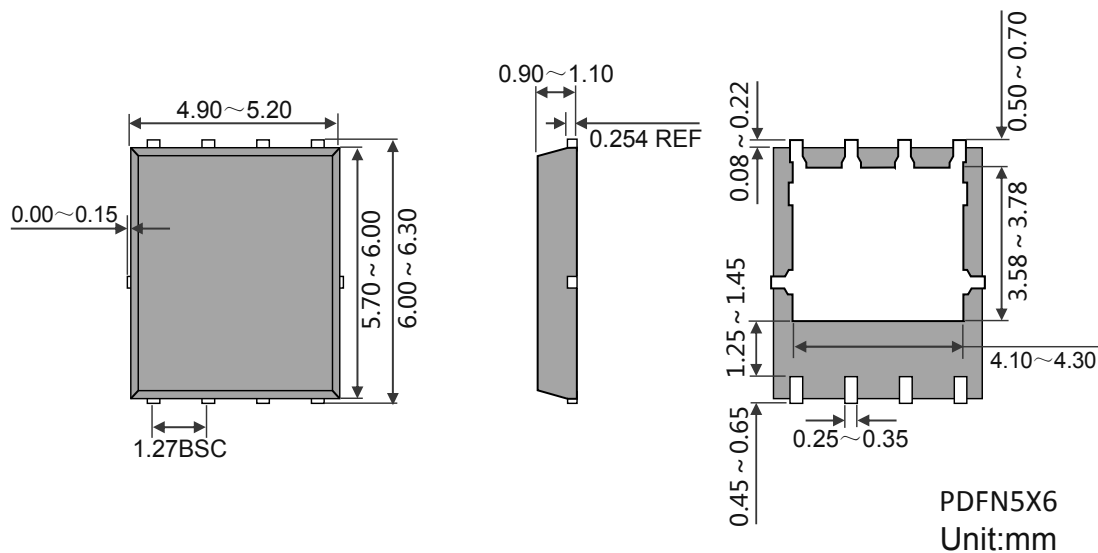
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



PDFN5X6 Package information



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